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PRELIMINARY SURFACE-EMITTING LASER LOGIC DEVICE EVALUATION

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13. ABSTRACT (Maximum 200 words)

This report discusses the evaluation of a monolithically integrated heterojunction phototransistor and vertical-cavity surface-emitting laser, designated the surface-Emitting Laser Logic device (CELL). Included is a discussion of the device structure and theory of operation, test procedures, results, and conclusions. Also presented is the CELL's opto-electronic input/output characteristics which includes spectral analysis, characteristic emitted light versus current and current versus voltage curves, input wavelength tolerance, output wavelength sensitivity to bias current, and insensitivity to input wavelength and power within a specified range.

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PREFACE

The surface-emitting laser logic device described herein was designed and developed by Photonics Research, Inc. (PRI) of Boulder, CO as a Phase I SBIR effort funded by SDIO. PRI performed the initial evaluation on the CELLs, and G. R. Olbright provided technical support for Rome Laboratory testing through discussions and assistance in data analysis. All Rome Laboratory and Cornell University work was split between S. I. Libby, P. D. Swanson, and M. A. Parker. S. I. Libby performed the experiments and wrote this technical report. P. D. Swanson and M. A. Parker assisted with the data analysis and experimental setup.

INTRODUCTION

Current electronic devices are reaching the physical limits for speed. Through optical processing, these limits can be overcome using massively parallel architectures.[1] Such processors require arrays of unique components to absorb and emit light vertical to the array's surface. One such promising component is the surfaCe-Emitting Laser Logic (CELL) device (figure 1). This photonic switching device consists of a monolithically integrated heterojunction phototransistor (HPT) and vertical-cavity surface-emitting laser (VCSEL), previously studied under hard-wired conditions.[1-3] The phototransistor receives light from an input source and provides the necessary current to drive the vertical-cavity laser above threshold. The input light can be from a single source or multiple sources. By controlling the power of the different inputs, the CELL can perform Boolean AND and OR operations.[1,3] Due to the phototransistor detector, the CELL has gain and can receive a wide range of input wavelengths, potentially converting incoherent light to coherent light.[2] The VCSEL as an output device provides a circularly symmetric output[4], a huge longitudinal mode spacing eliminating longitudinal mode hopping,[5] and a vertical (surface normal) output for ease of wafer-to-wafer interconnections. Reducing the reflectivity of the lower mirror allows optical feedback to the HPT providing the potential development as a memory element [2,6] as well as other logical functions.

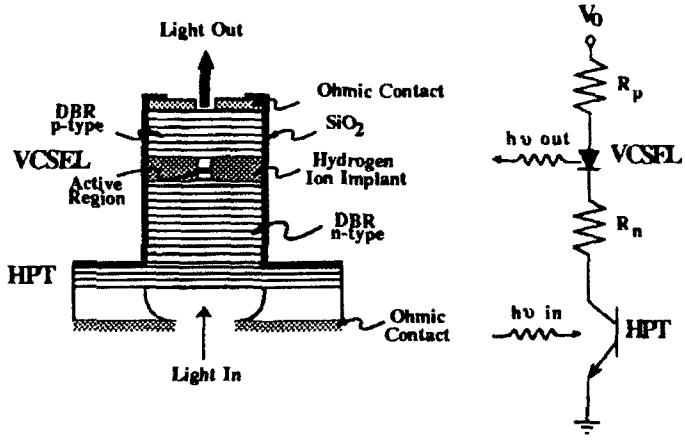

Figure 1: CELL Structure and Schematic Diagram[7]

This paper discusses the preliminary evaluation of the CELL. Component structure, fabrication, and theory of operation are first discussed; this is followed by the experimental procedures, results, and a discussion of the authors' interpretation of the results. Finally, we make some general conclusions and observations about the CELL and its future potential.

THEORETICAL BACKGROUND

Figure 1 shows the physical structure and a schematic representation of the CELL. This device consists of a VCSEL monolithically integrated with an HPT. Light is received by the HPT and emitted by the VCSEL. The CELL's structure and theory of operation are straight forward; its fabrication requires a number of processing steps.

As seen in figure 1, the VCSEL is fabricated on top of the HPT. Schematically, this portion of the CELL is represented by the diode and the two resistors (mirror resistances). The component parts of the VCSEL are the active region, the hydrogen ion implant region, the distributed Bragg reflectors (DBR), and the ohmic contact. The active region consists of GaAs-AlGaAs quantum wells. The hydrogen ion implants channel the drive current through the active region in a confined area. The DBRs are 18 to 30 periods of AlAs-AlGaAs 1/4λ stacks forming the Fabry-Perot cavity for the laser. The annular ohmic contact at the top of the VCSEL structure provides an output aperture for light emission. The SiO_2 layer indicated in the figure is used for side-wall passivation and was not present in the devices tested at Rome Laboratory. This structure serves as the light emission portion of the CELL.

The CELL's photo receiver is the HPT. This is a phototransistor which absorbs a wide range of optical wavelengths in its base and collector regions. With the proper amount of light absorbed by the base and collector, current flows from the collector to the emitter. This device operates as an NPN transistor in a common-emitter configuration with the input light acting as the source of base current, i.e. floating base configuration. A small amount of photo-generated current results in a large collector current which flows through the VCSEL structure. Therefore, as the light to the base of the HPT is increased, the collector current increases, and the VCSEL is brought above threshold, initiating laser operation.

The CELL is composed of varied layers of materials with various thicknesses. Specifically, from the substrate up, the layers deposited forming the HPT are the emitter, base, collector and sub collector, and the VCSEL layers are 25 to 30 periods of 1/4λ AlAs-AlGaAs to form the lower, high-reflection mirror, multiquantum wells of GaAs-AlGaAs for the active region, and finally, 18 to 25 more periods of the

AlAs-AlGaAs to form the top mirror output coupler. This as-grown structure is then masked, implanted, and etched to form the complete CELL structure.

Fabrication requires many different steps of masking, deposition, and etching[7] (figure 2). In step 2, a layer of photoresist (PR) is spun on but not patterned and a seed layer of gold is deposited on top. A second layer of photoresist is spun on, patterned, and developed normally to define the ion implant and top ohmic contact region. To achieve the structure in step 3, the sample is electroplated with gold, the top PR layer is removed, the exposed gold seed layer is wet etched, and the exposed lower PR surface is removed using reactive ion etching (RIE). Step 3's structure is then ion implanted down to the active region and the top ohmic contact is deposited, resulting in step 4. In step 5, the lower PR layer is removed using normal liftoff techniques. Next, the structure is masked (step 6) for reactive ion etching down through the HPT layers (step 7). This completes the top-side processing.

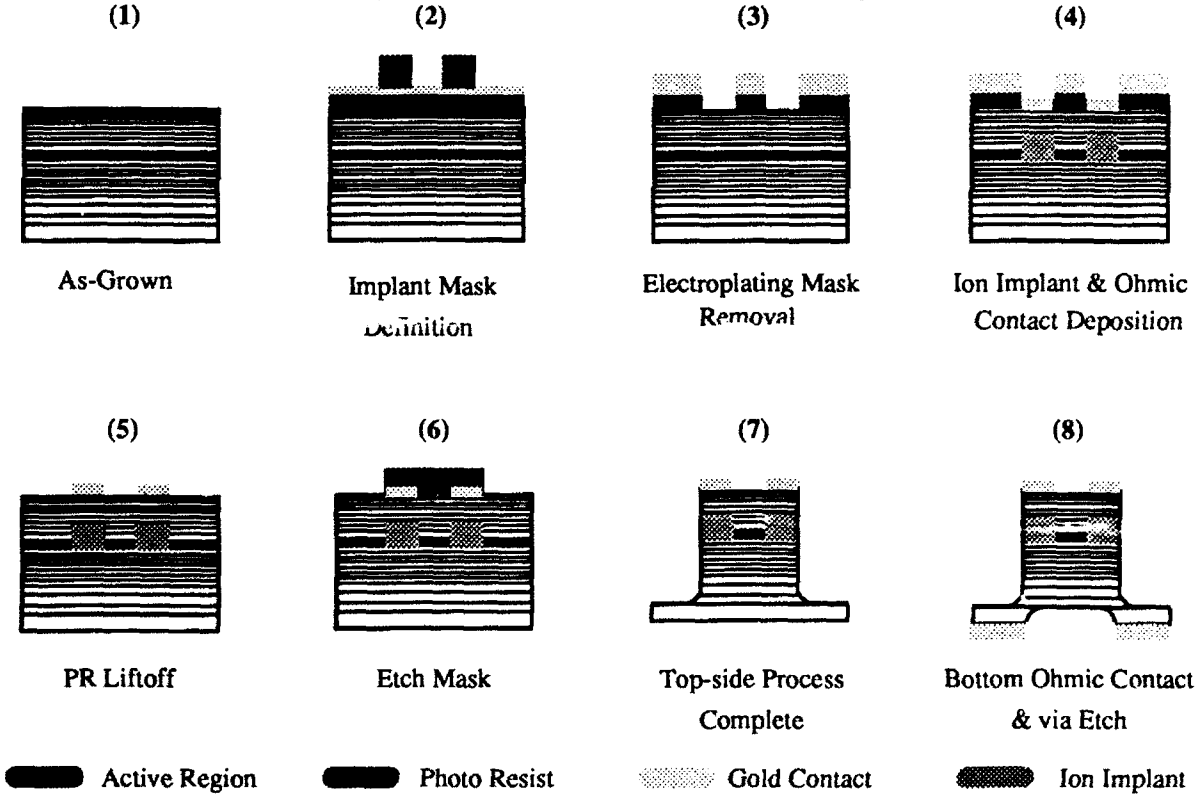

Figure 2: Fabrication Process

The bottom-side requires processing to form the lower ohmic contact and to open the *via* for the HPT input aperture. An IR source is projected through the wafer to accomplish bottom-side pattern alignment.

The ohmic contact and via patterning uses standard liftoff techniques. Finally, the substrate is etched up to the emitter portion of the HPT. The completed CELL structure appears as in Step 8.

EXPERIMENTAL PROCEDURES

Tests on the CELL required some modification to the setups used previously here at Rome Laboratory[8]. Because of its physical structure, the CELL requires electrical connections to its emitting surface which poses a problem with electrical probe placement. To eliminate this problem, a 45^{O} mirror is placed to reflect the device image upward (figure 3). This allows viewing of the output aperture and of the probe alignment. Electrical biasing and voltage/current measurements are performed using the Keithley 238 High-Current Source Measurement Unit (SMU). Optical power measurements are made by placing the optical power meter head between the mirror and the viewing microscope. Spectral analysis is performed using an optical fiber probe and the Anritsu MS9701B Optical Spectrum Analyzer (OSA).

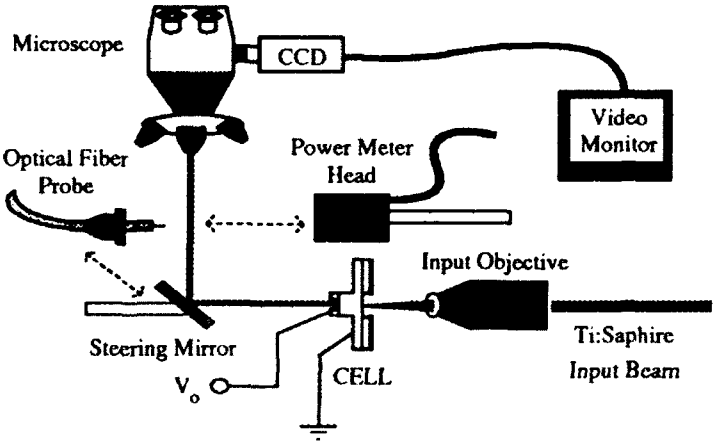

Figure 3: Probe Station Modifications for CELL Testing

CELL testing requires a multi-step alignment process. The first step is to align and place the electrical probes. Microscopic observation is used for physical probe placement. Electrically, the probes are connected to a curve tracer to determine when contact is made. Once proper probe placement is accomplished, the input optical beam is aligned with the input aperture on the backside of the CELL. Gross beam alignment is possible because of gaps present between the edges of the CELL chip and the package on which it is mounted. The input beam is aligned to pass through one of these gaps and is positioned so that only an X-axis translation is necessary for proper alignment. The beam is first roughly

focused by moving the [illegible] beam objective and observing it on the CCD camera display. The beam is then translated in the X-direction while observing the display on the curve tracer. As light strikes the CELL input, the I-V curve jumps up. At this point, adjusting the X-Y-Z position of the input objective maximizes the photo current. Increasing the input power should result in a device current of 2 to 5 mA for the VCSEL to lase.

Specific tests performed on the CELL are current versus voltage (I-V), emitted power versus current (L-I), and spectral analysis. The I-V and L-I tests are easily performed at the same time. First, the microscope is translated so the CELL under test is centered on the monitor's display. Next, the power meter head is placed above the mirror and aligned such that the light from the microscope is centered on its backside. Finally, the head is moved down as close as possible to the test setup without disturbing any of the components. The L-I-V test is computer controlled to place a bias across the device, measure the current and power, remove the bias from the device, change the bias level, and repeat at the new bias level. The test is performed automatically with input parameters of: on time, off time, minimum voltage, maximum voltage, compliance current (limit), and voltage step size. By varying the input wavelength and power the device's response range is observable.

The setup for the spectral response is more complicated. The probe connections and input light alignment are achieved as above. Once the CELL is connected and working properly, the 45^{O} mirror is replaced by the optical fiber probe. Any significant vibration can remove the CELL's electrical connections. Consequently, the I-V curve must be monitored throughout the entire alignment process to ensure electrical contact is maintained; otherwise, the mirror must be reinserted and the connections remade. Gross optical probe alignment is achieved visually, using the microscope for vertical and proximity alignments. Fine alignment is accomplished using a detector connected to a digital voltmeter. The CELL is DC biased with enough light input to generate a few milliamps of current. The optical probe is translated to get the peak voltmeter reading and then the microscope is used to place the probe tip as close as possible to the CELL's output aperture. The fiber is then connected to the OSA for spectral analysis. Again, the input light is varied to determine the CELL's response. Once the I-V, L-I,

and spectral data are obtained, the curves are analyzed to determine the CELL's response to varying input optical power, input optical wavelength, and DC bias current.

RESULTS AND DISCUSSION

Detailed analysis of the CELLs requires evaluation of their L-I/I-V curves and their spectral response. The CELLs were set up for L-I-V measurements with varying input powers and wavelengths. The spectral analysis setup measured the output wavelength versus bias current and input wavelength. All Rome Laboratory testing was essentially performed under DC conditions.

Initial Rome Lab CELL testing showed the need for the SiO_2 side-wall passivation. Even with input powers exceeding 5 mW, the maximum current through the device was on the order of 180 μA. This is far below the threshold needed to make the VCSEL lase. Figure 4 compares the I-V curve of a typical CELL obtained by PRI during the initial testing on 27 FEB 92 and that obtained at Rome Lab on 14 SEP 92. The CELL tested at RL only passes 90 μA at 6 V, while the data taken earlier show ≈ 2 mA at 6 V. The initial plot displays an operating resistance of 326 Ω, while the later operating resistance is approximately 64 kΩ. The problem is most likely due to oxidation of the de ice walls, causing a high series resistance. The high resistance inhibits sufficient current levels for laser operation. This problem was eliminated through a burn-in procedure. To remove the oxidation, a 1 mW optical input is applied to the phototransistor and the applied voltage is raised very high (≈ 16 to 18 V). The current is limited to 10 mA to prevent device destruction when the oxidation burns out. Gradually, as the oxidation is removed, the voltage necessary to reach the 5 mA level drops down to the 10 to 12 V range.

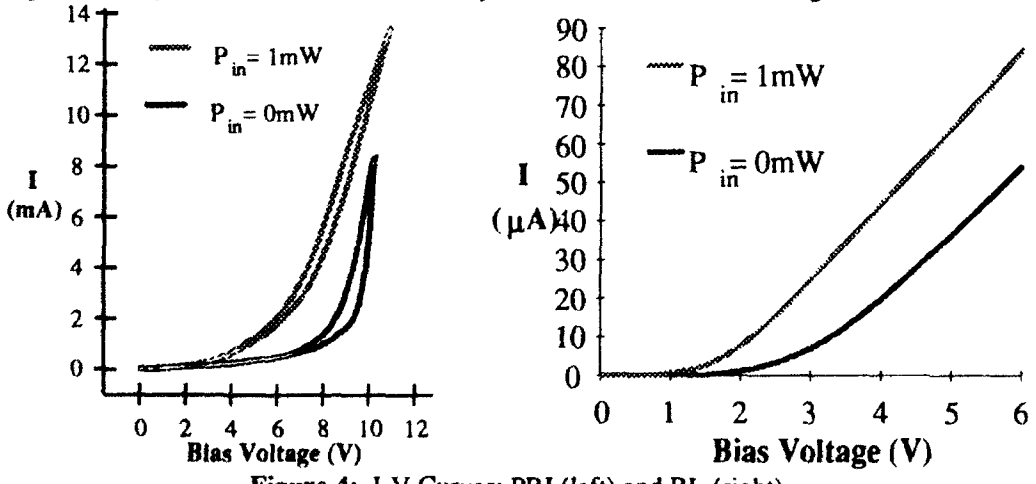

Figure 4: I-V Curves: PRI (left) and RL (right)

After the burn-in process, the CELL typically shows the L-I-V characteristic in figure 5. This CELL has an operating voltage of approximately 9 V. Extrapolating the L-I curve's linear portion gives a differential efficiency of 1.14 mW/A and a threshold current of 2.2 mA. The output power saturates at 0.75 μW due to the HPT-VCSEL interaction. This power is 1000 times lower than reported by PRI and indicates that the burn-in procedure is not completely successful. The linear portion of the I-V curve indicates an operating resistance of 186 Ω. This high resistance is due to the DBR mirrors and is a limitation of this device. The inset to figure 5 shows the spectral output of a different CELL with 1.75 mA bias and a 1 mW @ 850 nm input optical signal. This CELL's operating wavelength is 845.4 nm.

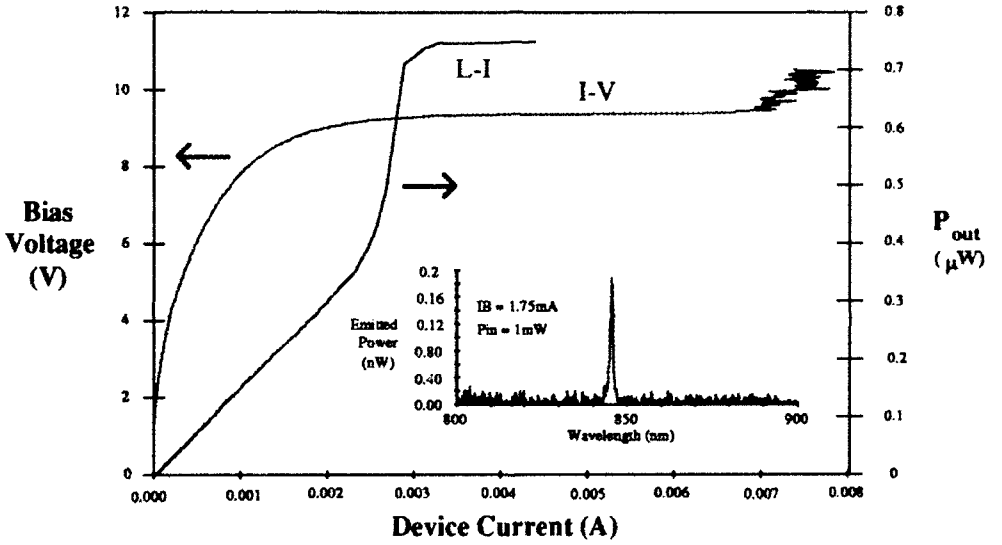

Figure 5: L-I-V Curve of a typical device. (Inset: typical emission spectrum.)

A properly operating CELL displays increased current with an increase in the optical bias signal. Photonic switching appears as an increase in the output power with an optical input beam present. The family of curves on the left (figure 6) indicates the transistor is working properly after the burn-in procedure. In this plot, as the optical input power is increased the amount of current through the device increases; i.e., increased input optical power turns the transistor on more, and therefore, more current flows. Once this current is in the 2 to 5 mA range, it is sufficient for the VCSEL to lase. The plot on the right shows CELL switching with input optical power. With no light input to the phototransistor, the output is 0.1 μW. When the input beam is applied, the output reaches 0.75 μW. This is a 7.5 to 1 contrast ratio.

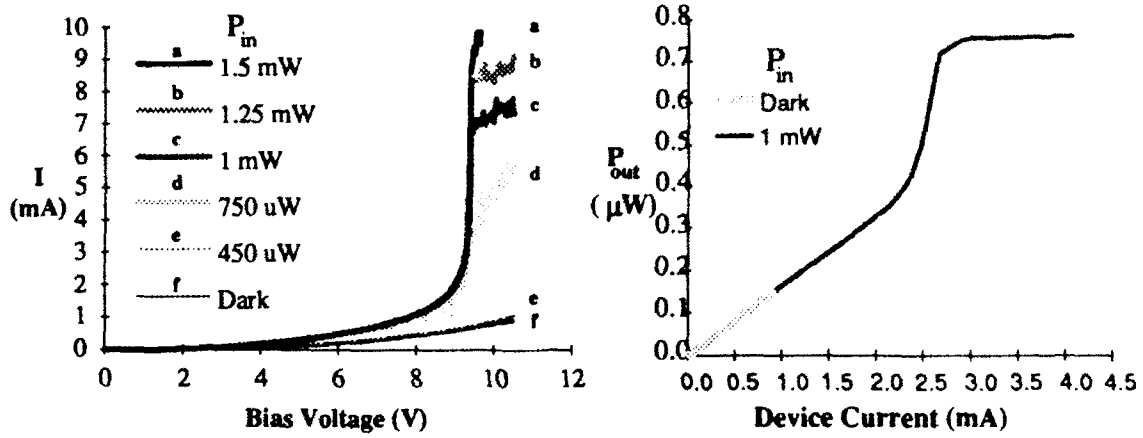

Figure 6: I-V Family Curve (Left) and Output Switching (Right)

In an operating optical processor it is reasonable to assume the operating conditions will fluctuate somewhat. Therefore, the CELL's response to changing inputs and bias conditions is critical. Figure 7 shows a given CELL's threshold current variance with changing optical inputs. These data are obtained by varying the input power (figure 7, left) and the input wavelength (figure 7, right), plotting the respective L-I curves, and extrapolating the threshold current from each. The I_{th} versus P_{in} plot indicates that the threshold current does not vary with a change in input power. The I_{th} versus λ_{in} plot indicates that the threshold current is fairly constant with varying input wavelengths. Therefore, the threshold current is insensitive to fluctuations in the input optical power and wavelength.

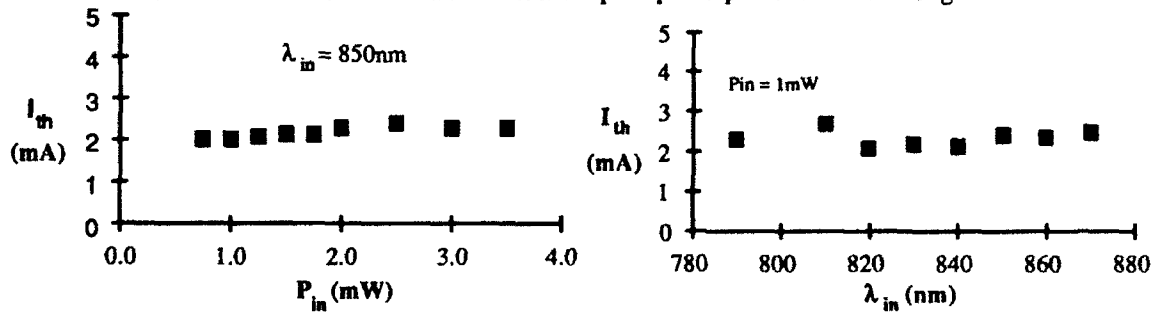

Figure 7: Threshold Current versus Input Power (Left) and Input Wavelength (Right).

Perhaps the most critical aspect of the photonic switching device is that its output remain stable despite input instabilities. Figure 8 shows plots of peak and integrated CELL powers with varying bias currents and input wavelengths. These data were taken from the OSA plots under the given conditions. The P_{out} versus I_B plot shows a definite dependence of the output power on bias current. This indicates there is an optimum current at which to operate; in this case that optimum current is 1.75 mA. With currents much above this, the output power starts to drop off due to heating. Therefore, device

temperature control is necessary. The P_{out} versus λ_{in} plot indicates there is no significant change in the output power with varying input wavelengths. The integrated power does start to rise for input wavelengths above 860 nm. This is due solely to the fact that the input beam wavelength is below the bandgap energy and is passing through the substrate, not absorbed. This is important to know when cascading these devices and determines a limit of about 860 nm for the input wavelength.

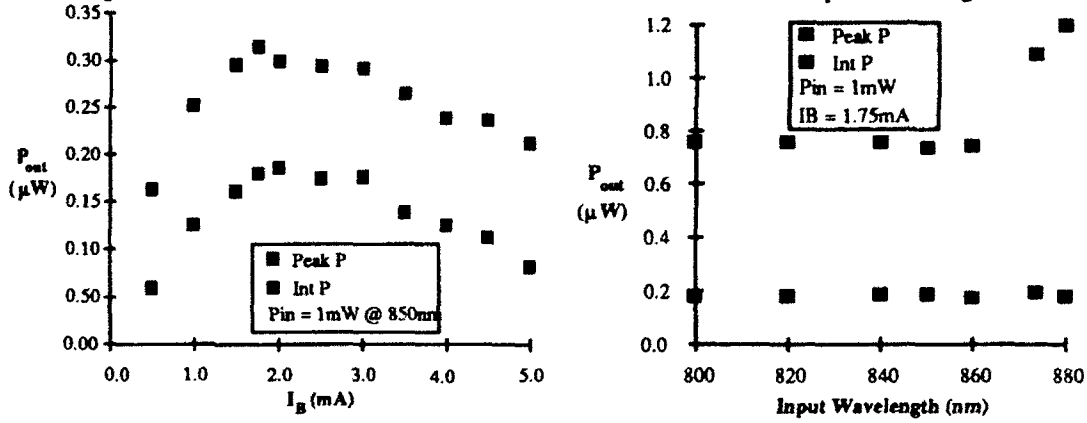

Figure 8: Peak/Total Power versus Bias Current and Input Wavelength
(Note: Power measurements are made by coupling the output signal to the OSA via a multimode fiber.)

The CELL's output wavelength stability for changing bias current and input wavelength is displayed in figure 9. The λ_{out} versus I_B plot shows a linear rise in the output wavelength with increasing bias current. The slope of this curve corresponds to 844 MHz/μA. Again, this is a direct indication of heating effects and of the need for temperature control. The λ_{out} versus λ_{in} plot indicates there is no variance of output wavelength due to input wavelength. Therefore, the CELL's spectral output remains constant despite the wavelength of the signal used to turn the CELL on, but temperature and bias current must be controlled to maintain a stable output wavelength.

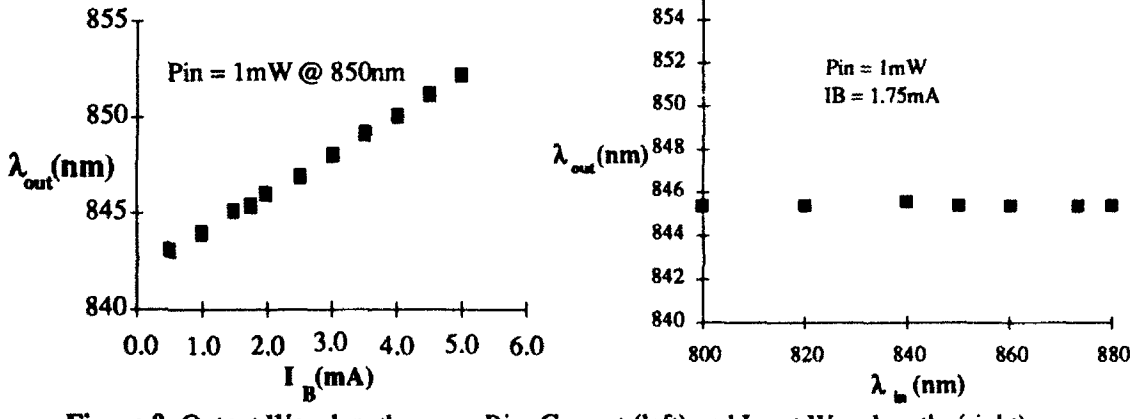

Figure 9: Output Wavelength versus Bias Current (left) and Input Wavelength (right).

One critical observation is that the HPTs are not isolated from one CELL to another on this chip; this is seen under two conditions. First, placing the V_O probe on the substrate results in a pn-junction curve on the curve tracer. Second, an observable change in the I-V curve occurs by biasing one CELL electrically and biasing a different CELL optically. This is a problem that must be corrected to make CELL arrays usable; otherwise, data crosstalk would eliminate the array's usefulness.

CONCLUSIONS

From the results presented here, the CELL works as a photonic switching device. With proper biasing, the VCSEL is turned on or off due to the input light. The CELLs saturate at approximately 750 nW resulting in an output contrast ratio of 7.5 under DC conditions. Typical bias voltages range from 9 to 12 V with on resistances of $\approx 200\ \Omega$ after burn in and operating wavelengths of 845 to 851 nm. The high resistance is due to the DBR mirror stacks and limits the usefulness of the CELL. However, PRI has recently succeeded in dramatically reducing the voltage threshold by incorporating a new design which avoids current flow through an upper p-type region[9]. This advancement in VCSEL technology, when incorporated into the CELL device, promises to significantly reduce ohmic heating and increase wall-plug efficiency. There was a significant difference in output power between the initial CELL tests and those that required burn in. This indicates that the burn-in process does not absolutely reverse the aging effects. As expected, threshold currents remain constant with changing input power and wavelengths. Output power is not dependent on input wavelength but is dependent on bias current; this is consistent with earlier reports.[10] The output wavelength is not dependent on the input wavelength but varies linearly as 1.87 nm/mA (844 MHz/μA) with bias current as compared to 130 MHz/μA reported for a VCSEL.[10] The indication here is that the CELLs are heating more significantly over a range of bias current.

Some general observations can be made which pertain to CELL testing. The device, as constructed, is not mechanically strong due to the deep etch at the top and the via etched in the bottom. For this particular set of devices, the HPTs are not electrically isolated. However, an array of CELLs configured in this way could be used to perform a massive OR operation. In this case, one particular CELL would be used as the array output, while all of the CELL inputs could be used to switch the output on. As seen,

the fabrication steps are long and complicated. The required double-sided processing makes mass production of these arrays difficult at best. Side-wall passivation is a necessity in order to maintain the reliability of the arrays over time. These are some of the factors which would control further development of the surface-emitting laser logic device in the transmission mode of operation. Consequently, future CELL work by PRI will be conducted in reflection mode to eliminate these problems. In addition to side-wall passivation, future developments might include changing the material of the HPT to operate at a longer wavelength such as reported by Bryan etal.[11] This would eliminate the need for the vias, which would make the device more mechanically stable and would provide for a larger margin of error when etching down through the HPT layers providing better electrical isolation. However, this approach requires, in one embodiment, use of a resonant cavity HPT combined with strained InGaAs quantum wells, making implementation difficult.[11] The CELLs described here are very versatile photonic switching devices; when modified and fabricated into arrays, they could provide the necessary basic building block for future digital optical processors.

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